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Semiconductor Surface Varactor

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The semiconductor varactor using surface space charge is analyzed and measurements made on several experimental units are described. The chief characteristics of this device are its capacity-voltage dependence and its negligible dc conduction.

The particular system used in this work is a thermally grown oxide on silicon. A theory developed from the surface charge relation is shown to agree with the experimental data over a wide range of silicon resistivity.

The theory for optimum operation for both dc and ac biasing is derived and used to compare the performance of this device with that of the p-n junction varactor. The result of this comparison shows that with careful design the semiconductor surface varactor will be able to compete favorably with the junction varactor for many possible applications, including those of ultra high frequency.

I. INTRODUCTION

In recent years semiconductor p-n junctions have found wide use in parametric amplifiers, harmonic generators, and frequency modulators. These applications result from the fact that the space charge layer capacity of the junction is voltage dependent and thus easily variable.

Another semiconductor varactor which in some instances shows a greater dependence of capacity upon voltage has been investigated recently.[1,2] Unlike the junction varactor, the modus operandi of this new device is the change of the distribution of charge at a semiconductor surface with an applied normal field. Since the surface in a sense replaces the junction, the device has been termed a "surface varactor." The device has also been termed an "ON varactor" (for *o*xide-*n*-silicon) and an "MOS diode" (for *m*etal-silicon *o*xide-silicon).

The structure is shown in Fig. 1. It consists of an insulator (across which the normal field is applied) in intimate contact with a semiconducting material. The silicon-silicon dioxide system was used in all our experiments.

II. QUALITATIVE DESCRIPTION

A qualitative description of the basic principles of the surface varactor is helpful in understanding the more detailed theory. This discussion makes use of the surface varactor as shown in Fig. 1 with p-type silicon. In this discussion, the capacity corresponds to that which would he measured with a negligibly small ac signal in conjunction with the indicated dc bias voltage.

1. Consider that a negative voltage is applied to the contact on the oxide, which we will call the "field plate." Holes from the interior of the silicon hody are attracted toward the silicon-silicon dioxide interface, resulting in an enhancement or accumulation of charges. These holes, which are located close to the interfacc, form a charge layer of negligible thickness, equal and opposite to the chargc layer on the field plate. Thus, as is shown at point A of Fig. 2, the capacity is that due to the oxide alone.

2. If, on the other hand, the field plate voltagc is slightly positive, holes are repelled from the interface leaving exposed ionized accceptors. The charge layer in the silicon composed of these ionized acceptors thus extends to a relatively large depth, which effectively increases the distance between it and the charge layer at the field plate. The capacity is therehy reduced from the value of the oxidc capacity as indicated hy point B in Fig. 2. The charge distribution approaches that of a reverse-biased n^+p step junction.

3. Increasing the positive voltagc still further will eventually begin to accumulate a suhstantial density of generated electrons at the interface, resulting in an inversion condition of charge; i.e., the surface charge

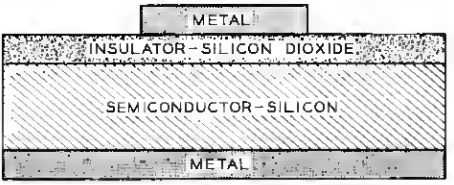

FIG. 1 — Schematic illustration of the surface varactor showing the oxide layer on one side of the silicon wafer and the metal contacts.

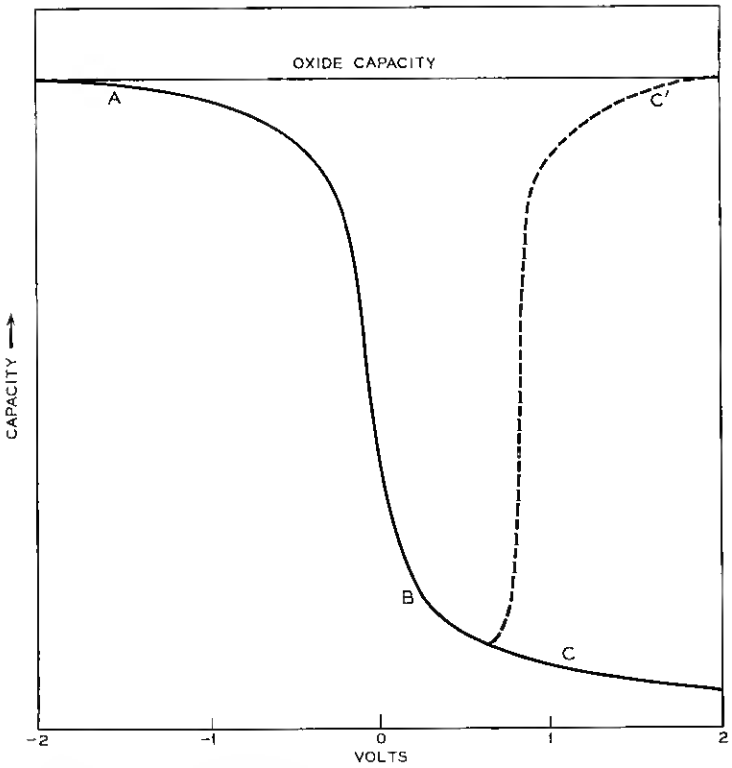

FIG. 2 — Curve ABC is a typical capacity vs voltage curve for a surface varactor. Curve ABC′ is a special case.

is now opposite in sign to the normal bulk carriers. However, this effect of electrons on capacity becomes pronounced only when their density becomes as large as that of the acceptor density. At sufficiently high bias the space charge will be predominately made up of electrons, again in a relatively narrow region near the surface, and the capacity will approach the oxide capacity as a limit. This is shown by the dashed line BC′ of Fig. 2. To obtain this increase in capacity, which is due to change in density and distribution of electrons (minority carrier), one must carry out the measurement at sufficiently low frequency to provide the necessary time for generation and recombination of the electrons. If, on the other hand, the measurement is carried out at higher frequencies, the above rate of the electrons and the increase in capacity with bias is not obtained. Instead, the change in charge within the space charge will be made up entirely of fixed acceptor charges. The capacity will then con-

tinue to decrease with applied bias as shown by point C of the solid line of Fig. 2. This decrease (B–C) however, is appreciably smaller than that of a reverse-biased n^+p junction. This is because, at a given dc bias, the generated minority carriers (electrons) are accumulated in the surface varactor case, while in the case of the n^+p junction they are swept away. One obtains, therefore, a narrower space-charge region for the surface varactor than for the n^+p junction with this method of biasing.

The frequency ranges in which the capacity will increase or decrease depends on the magnitude of the ac signal, the carrier lifetime, and the semiconductor resistivity. However, for silicon, using reasonable values of these parameters (ac signal >10 mv, lifetime $>10^{-9}$ sec., resistivity <1000 ohm cm) at frequencies of about 10,000 cps and above the capacity will decrease.

III. METHOD OF APPLYING BIAS

In the preceding discussion the bias has been described as a dc bias. This meant that the bias was manually applied in steps and the capacity was measured with an ac signal of negligible magnitude as in Fig. 3(a). The case will be referred to as the "dc-bias case." All experimental results were obtained in this manner. However, another important method of biasing will also be discussed. This is the use of ac biasing, which is necessary when using the device as a parameter amplifier or harmonic generator. For purposes of determining the capacity variation, an additional higher frequency ac signal of small magnitude is assumed as in

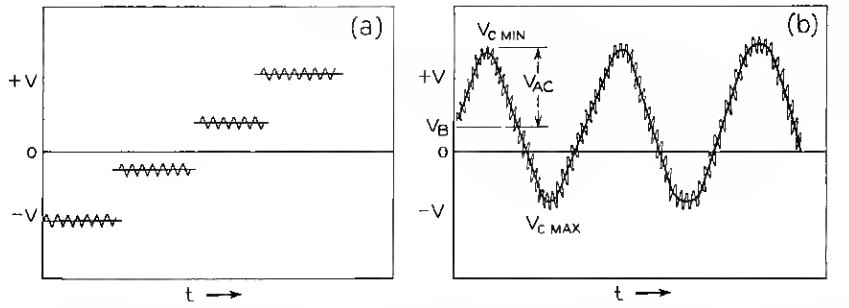

FIG. 3 — Methods used in biasing surface varactor. (a) DC biasing — dc voltage is stepped to each value and small ac signal is used to measure the capacity at each voltage step. (b) AC biasing — bias is made up of a dc component V_B (+ for p-type silicon, − for n-type silicon), and an ac component, V_{ac}; a small higher frequency ac signal is used to measure the capacity at any point. The capacity ratio is defined as C_{max}/C_{min}.

Fig. 3(b). (Note that there can be a dc component to the ac bias.) This case will be referred to as the "ac-bias case."

With this background, the analysis of the problem is carried out as presented in the following order.

First, the relations between the equilibrium charge and the voltage across the device are presented. This leads to a general expression for the capacity.

Next, relations are derived for dc-bias case. These relations are then compared with the experimental results for several silicon resistivities. Also, curves are presented to show the highest capacity changes possible with a dc bias.

The ac-bias case is then analyzed and the proper biasing to obtain the optimum capacity changes are determined.

A relation for minimum cutoff frequency is derived and compared with experimental values. Cutoff frequencies obtainable with very thin epitaxial films are calculated. Experimental results of the effect of temperature are also shown.

In the last sections a comparison is made between the performance of the surface varactor and that of the junction varactor. Finally a brief comment is made for the case where the silicon resistivity shows a gradient from the surface.

IV. BASIC THEORY — EQUILIBRIUM CHARGE RELATIONS

The theory of the surface varactor is an extension of the fundamental theory of the space-charge region at the surface of a semiconductor

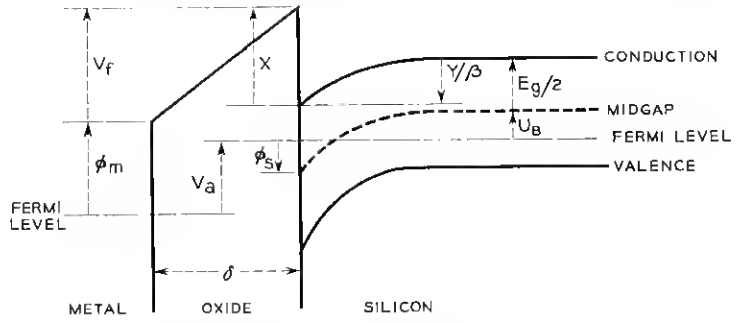

FIG. 4 — Potential diagram that exists across the metal-oxide-silicon surface. Although the equation derived from it is quite general, this diagram is specifically for a p-type silicon biased so the silicon surface at the oxide interface has inverted. The direction of the arrows refers to the positive value of the potentials.

when an external electric field is applied.[3] The band picture that governs in this case is shown in Fig. 4. In general, a voltage across the device, V_a, is associated with charge in both the space-charge region and the surface states. In equilibrium these charges are given[3] by the relations

$$Q_{sc} = \pm en_i\mathfrak{L}[\lambda(e^{-Y} - 1) + \lambda^{-1}(e^{Y} - 1) + (\lambda - \lambda^{-1})Y]^{\frac{1}{2}}$$
$$(-) \quad \text{for} \quad Y > 0, \qquad (+) \quad \text{for} \quad Y < 0, \quad (1)$$

where

e is the electron charge
n_i is the intrinsic density of electrons
$\mathfrak{L}$ is twice the Deybe length
λ is the doping density normalized to the intrinsic density
Y is the surface potential relative to the bulk in kT units

and

$$Q_{ss} = eF_{ss}(Y) \tag{2}$$

where the function $F_{ss}(Y)$ includes the density of surface states and their distribution within the energy gap. A third relationship can be determined directly from Fig. 4 by balancing potentials

$$V_a = \varphi_m - (\chi + u_B + E_g/2) + V_f + Y/\beta \tag{3}$$

where

V_a is the applied voltage
φ_m is the work function of the metal
χ is the electron affinity of the semiconductor
u_B is the bulk potential difference of midgap to Fermi level
E_g is the energy gap

and

V_f is the oxide film voltage

and also

$$Q = Q_{sc} + Q_{ss} = C_f V_f \tag{4}$$

where

Q is the total charge and
C_f is the capacity of the oxide film.

The general relation for the capacity of the structure under any con-

dition is

$$C = \frac{dQ}{dV_a} = \beta \frac{dQ}{dY} \frac{d(Y/\beta)}{dV_a}.$$

Then, by differentiating (3) and (4),

$$C = \frac{C_{si}C_f}{C_{si} + C_f} \tag{5}$$

where

$$C_{si} = \beta \frac{dQ}{dY}. \tag{6}$$

This relation corresponds to separate capacitors in series, one being the oxide film capacity and the other an effective silicon capacity. One must be careful, however, in applying this concept of series capacitors. It is *not*, for instance, completely equivalent to the case of a p-n junction capacitor in series with a linear capacitor. In this latter case two sets of positive and negative charges are encountered, one on the p-n junction and the other on the series capacitor. In the surface varactor, on the other hand, *only one* set of positive and negative charges is present.

V. DC-BIAS CASE

When true equilibrium is maintained, differentiation of (1) and (2) would suffice to determine the capacity explicitly. The result of this is

$$C_{si} = C_{sc} + C_{ss}$$

where

$$C_{sc} = \beta \frac{dQ_{sc}}{dY} = \frac{\epsilon_{si}[\lambda(1 - e^{-Y}) - \lambda^{-1}(1 - e^{Y})]}{\mathfrak{L}[\lambda(e^{-Y} - 1) + \lambda^{-1}(e^{Y} - 1) + (\lambda - \lambda^{-1})Y]^{\frac{1}{2}}}$$

ϵ_{si} being the dielectric constant of silicon, and

$$C_{ss} = \beta \frac{dQ_{ss}}{dY} = \beta F_{ss}'(Y).$$

Curve ABC′ with the dashed portion C′ of Fig. 2 was calculated using the above relation, setting $C_{ss} = 0$.

However, as discussed previously, equilibrium is not normally attained in the useful frequency range. We will now calculate the capacity-voltage characteristic of a surface varactor subjected to a dc bias and an ac signal sufficiently rapid that minority carriers cannot equilibrate

within the duration of an ac cycle. In this analysis, the surface states are also assumed to be unable to equilibrate, hence $C_{ss} = 0$ and $C_{si} = C_{sc}$. The analysis is presented in the Appendix. The results are:

for p-type

$$C_{si} = \frac{\epsilon_{si}\lambda^{\frac{1}{2}}(1 - e^{-Y})}{\mathfrak{L}(e^{-Y} - 1 + Y)^{\frac{1}{2}}}, \text{ for } Y - 1 > e^{Y}\lambda^{-2}*$$
$$C_{si} = \frac{\epsilon_{si}\lambda^{\frac{1}{2}}\mathfrak{L}^{-1}(y_1 - 1)^{\frac{1}{2}}}{y_1 - e^{-\frac{1}{2}}(Y - y_1)}, \text{ for } Y - 1 < e^{Y}\mu^{-2} \tag{7}$$

where y_1 is defined by

$$y_1 - 1 = e^{y_1}\lambda^{-2}.$$

Physically, when the surface potential is y_1, the charge due to minority carriers is about equal to the fixed charge.
For n-type

$$C_{si} = \frac{\epsilon_{si}\lambda^{-\frac{1}{2}}(1 - e^{Y})}{\mathfrak{L}(e^{Y} - 1 - Y)^{\frac{1}{2}}}, \quad \text{for } -Y - 1 > e^{-Y}\lambda^{2}$$
$$C_{si} = \frac{\epsilon_{si}\lambda^{-\frac{1}{2}}\mathfrak{L}^{-1}(-y_1 - 1)^{\frac{1}{2}}}{-y_1 - e^{\frac{1}{2}}(Y - y_1)}, \quad \text{for } -Y - 1 < e^{-Y}\lambda^{2} \tag{8}$$

where y_1 is defined by

$$-y_1 - 1 = e^{y_1}\lambda^{2}.$$

The complete theoretical small-signal capacity vs voltage relation can be calculated from (1), (2), (3), (4), (5), and (7) or (8). The procedure is to list values of Y and determine the capacity and voltage common to each value of Y. It is seen from (3) and (4) that surface states, Q_{ss}, and work function difference, $\varphi_m - (\chi + u_B + E_g/2)$, can cause an additive constant to the applied voltage V_a. Nonzero values of Q_{ss}, however, can also cause more complex capacity variation with voltage. Calculations for several resistivities, assuming work function difference and Q_{ss} to be zero, are plotted as dashed lines in Figs. 5 and 6.

VI. EXPERIMENTAL COMPARISON OF THEORY

Units were fabricated using silicon of 15 ohm cm — p-type, 15 ohm cm — n-type, 0.2 ohm cm — n-type, and 0.029 ohm cm — n-type.

* For $Y = 0$, $C_{si} = \frac{\epsilon_{si}}{\mathfrak{L}}\sqrt{2\lambda}$.

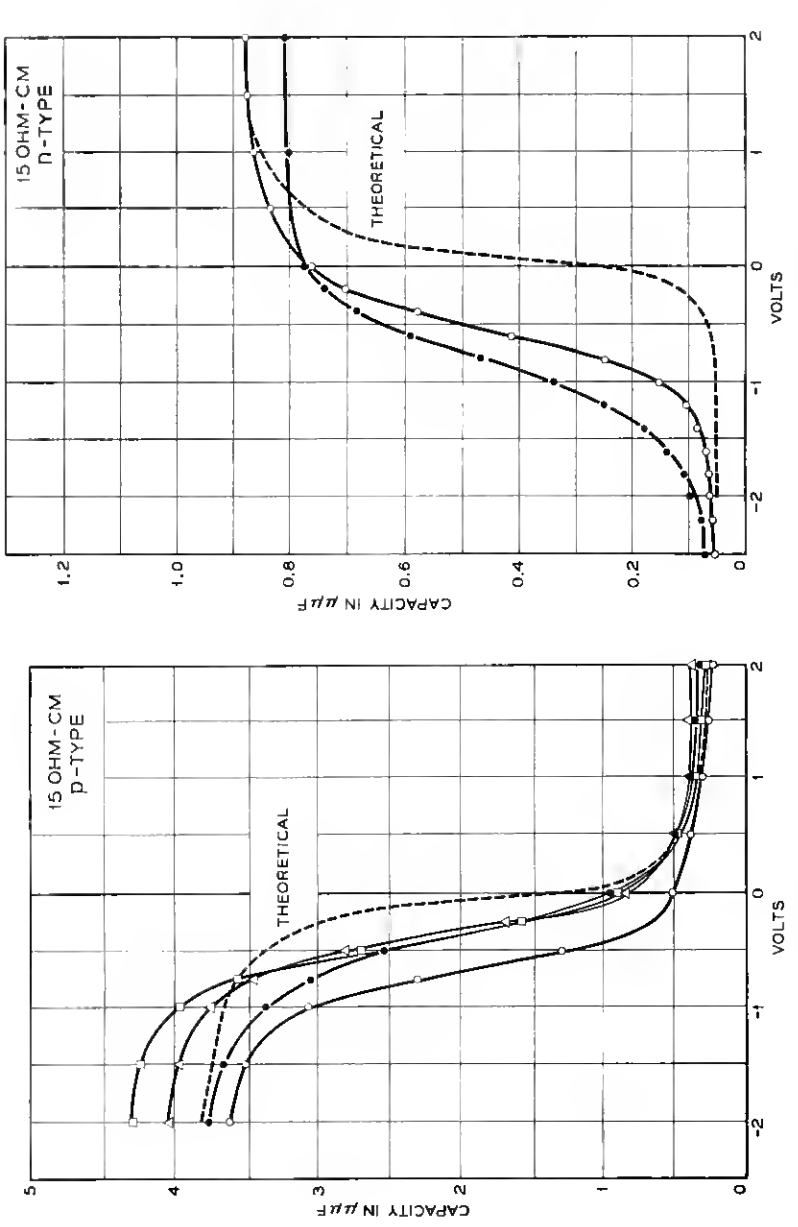

FIG. 5 — Solid lines are experimental plots of the capacity measured over a range of bias voltage. The results of four units made from 15 ohm cm p-type silicon are shown on the left and two units of 15 ohm cm n-type silicon are shown on the right. The measurements were made with a 30 mv, 100,000 cps signal. The dashed lines are the theoretical curves for the quasi-equilibrium case (assuming no surface states) described in the text.

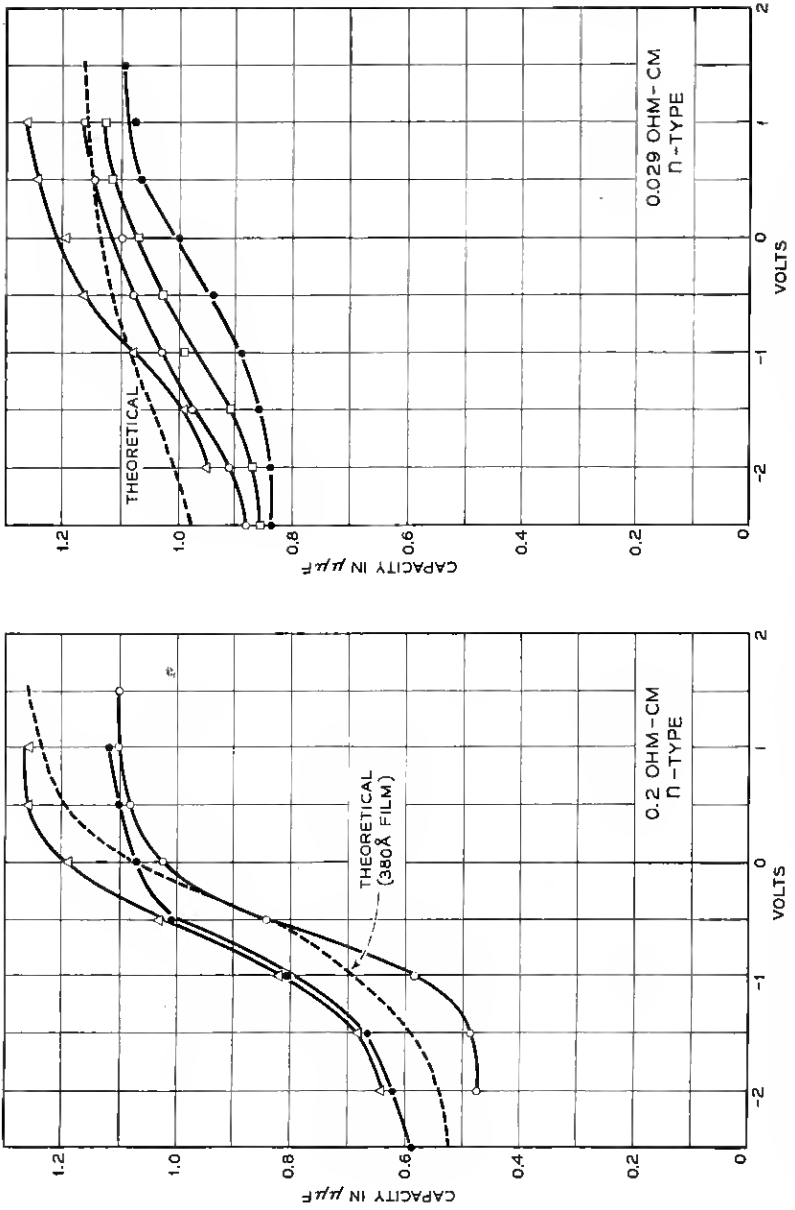

FIG. 6 — Similar to Fig. 5 except units on left were made from 0.2 ohm cm n-type silicon and those on the right are 0.029 ohm cm n-type.

The technique used was to etch the silicon slice to 0.004 inch, evaporate a metal contact on one side, and further etch the working surface to a final thickness of 0.002. The slices were then etched into 0.040 inch diameter discs and subsequently cleaned and thermally oxidized[4] at 920°C for 30 minutes. The oxide thickness ranged from 300 Å to 400 Å, and the active or contact area, obtained by pressing a gold point on the oxide, ranged from 1 to 3×10^{-5} cm^2, or about a 2 mil diameter.

The capacity versus voltage measurements of several experimental units with a 100,000 cps, 30 mv signal are presented in Figs. 5 and 6, along with the theoretical quasi-equilibrium curves (by "quasi" it is meant that the minority carriers do not reach equilibrium — curve C of Fig. 2 instead of C′). The shape of the capacity-voltage curves agrees reasonably well with the theoretical curves. Except for the 0.029 ohm cm case there is a uniform voltage translation to negative values of 0.2 to 0.7 volts. Considering the surface states[4] to be at the oxide-silicon interface, if the work function difference is zero, this voltage corresponds to a particular charge (residing in the surface states) on the oxide capacity. Thus for a voltage translation, V_{ss}, $Q_{ss} = V_{ss}C_f$, which for 0.7 volts and a 300 Å film corresponds to a donor surface state density of 5×10^{11}/cm^2.

VII. VARACTOR QUALITY

Two quantities of importance for the performance of a varactor are the ratio between the maximum and minimum capacities and the cutoff frequency. Various figures of merit have been proposed that usually combine these factors in various ways. The cutoff frequency is of greatest importance in high frequency amplifiers, while the capacity ratio is important throughout the frequency range.

VIII. MAXIMUM CAPACITY RATIO

8.1 *DC-Bias Case*

The magnitude of capacity change with bias is given by the ratio (C_{max}/C_{min}). C_{max} is generally limited by and identically equal to the oxide film capacity, C_f, and C_{min} is determined by the space-charge capacity (which is a monotonically decreasing function with bias) but is limited by the maximum field, E_f, allowed on the oxide.* The field

* This field could also be limited by Zener breakdown of the silicon for very low resistivities ($\rho < .01$) but these resistivities normally produce negligible capacity change for this structure.

must be limited to this value since dielectric breakdown of the oxide is destructive. Using (5)

$$\frac{C_{\max}}{C_{\min}} = 1 + \frac{C_f}{C_{si_{\min}}}. \tag{9}$$

The relation between the maximum field, E_f, and the maximum band bending, Y_M, is given by (1) with $e^Y \gg \lambda^2 Y$ and is

$$Y_M = 2 \ln \frac{\epsilon_f E_f \lambda^{\frac{1}{2}}}{e n_i \mathfrak{L}}.$$

Then to find $C_{si_{\min}}$ this value of Y_M should be substituted for Y in (7). It can be shown, however, that for $E_f \geqq 10^6$ v/cm and $\lambda \leqq 10^8$, we have $Y_M > y_1$. Thus, closely

$$C_{si_{\min}} = \frac{\epsilon_{si} \lambda^{\frac{1}{2}}}{\mathfrak{L}} \frac{(y_1 - 1)^{\frac{1}{2}}}{y_1}$$

and substituting into (9),

$$\frac{C_{\max}}{C_{\min}} = 1 + \frac{\epsilon_f \mathfrak{L}}{\delta \epsilon_{si} \lambda^{\frac{1}{2}}} \frac{y_1}{(y_1 - 1)^{\frac{1}{2}}}.$$

This is plotted in Fig. 7 for a range of normalized doping density, λ, and oxide thickness, δ, using $E_f = 3 \times 10^6$ v/cm. Ratios of over a hun-

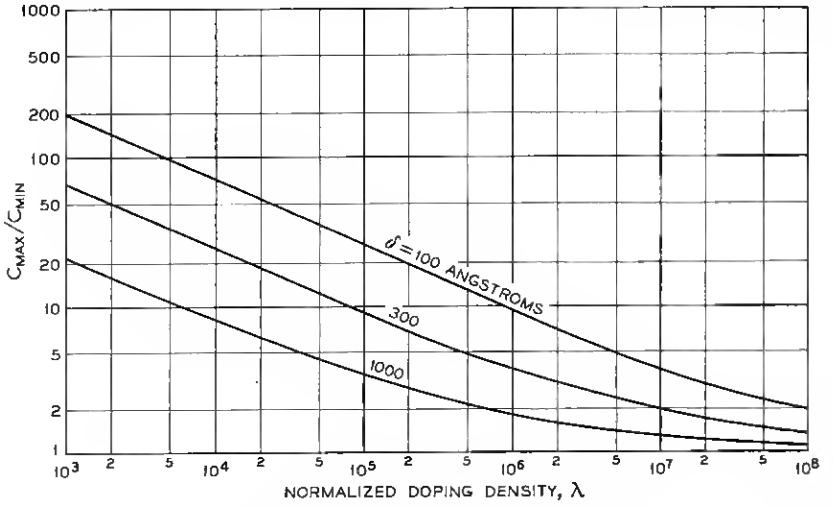

FIG. 7 — The maximum capacity ratio obtainable as a function of λ and oxide thickness for the dc-bias case. The maximum field on the oxide is 3×10^6 v/cm.

dred are possible with the high resistivity (low λ) material and decrease approximately as the one-half power of λ.

8.2 *AC-Bias Case*

An important mode of operation of the surface varactor is large ac bias signals superimposed on a dc bias voltage. Such conditions occur in low-noise variable capacitance amplifiers. Here we are interested in the variation of the capacity during the ac cycle rather than the variation of the capacity with dc bias as discussed for the dc-bias case (See Fig. 3). In this presentation we will assume minority carrier equilibration cannot occur during one period of the ac bias signal so that minority carrier charge is fixed at its magnitude at the dc component of the bias. Now when large ac biases are applied, the field must terminate on exposed fixed charges. Larger bending of the bands is obtainable than in the pure dc-bias case, without exceeding the oxide dielectric strength, because the density of minority carriers at the oxide-silicon interface is limited. This is shown by the following analysis.

The maximization of the dc and ac components of the bias to attain the greatest band bending is governed for either polarity of voltage by

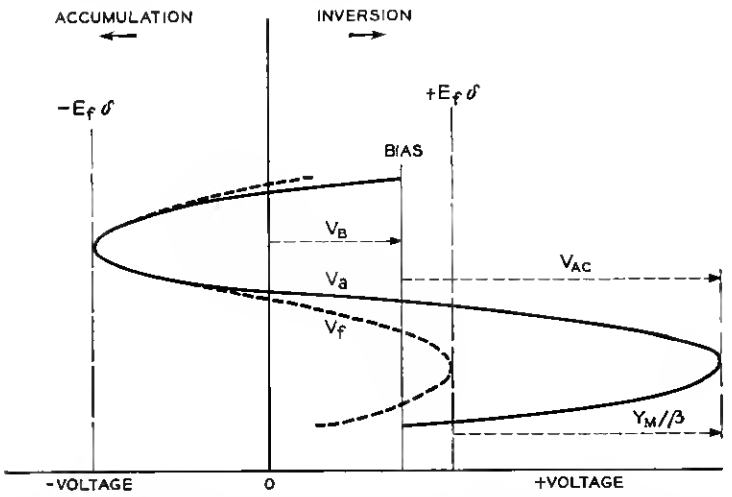

FIG. 8 — Representation of applied voltage in the ac-bias case. The solid curve is the applied voltage, V_a, which is a sine wave displaced from zero by the value of the bias voltage, V_B. The dashed curve, V_f, is the fraction of the applied voltage which is carried by the oxide film. The vertical dashed lines are the limits of voltage which can be safely carried by the oxide film. The diagram assumes p-type silicon.

the dielectric strength of the oxide. To avoid dielectric breakdown of the oxide when bending the bands toward accumulation, as seen in Fig. 8,

$$V_{ac} \leqq V_B + E_f\delta, \tag{10}$$

where V_B is the applied dc bias, and V_{ac} is the zero to peak value of the ac bias. And when bending the band toward inversion,

$$V_f = V_{ac} - \frac{Y_M}{\beta} + V_B \leqq E_f\delta, \tag{11}$$

where Y_M is the band bending at the peak value of the signal. For the greatest Y_M the equations are equalities. Solving (10) and (11)

$$V_{ac} = E_f\delta + \frac{1}{2}\frac{Y_M}{\beta} \tag{12}$$

and

$$V_B = \frac{1}{2}\frac{Y_M}{\beta}. \tag{13}$$

The charge in the space-charge region at the time of maximum bending is given by the sum of the minority carrier charges* plus the acceptor charges, the expressions for which can be obtained from the Appendix. Thus if $Q_{ss} = 0$

$$Q = Q_{sc} = \epsilon_f E_f = en_i\mathfrak{L}\lambda^{-\frac{1}{2}}e^{Y_B/2} + en_i\mathfrak{L}\lambda^{\frac{1}{2}}Y_M^{\frac{1}{2}}$$

where Y_B is the band bending at the dc bias voltage. Note that the electron charge is determined at the dc bias voltage. From which

$$Y_B = 2\ln\left[\frac{\epsilon_f E_f\lambda^{\frac{1}{2}}}{en_i\mathfrak{L}} - \lambda Y_M^{\frac{1}{2}}\right]. \tag{14}$$

The charge at the dc bias point is

$$Q = C_f V_f = \frac{\epsilon_f}{\delta\beta}\left(\frac{Y_M}{2} - Y_B\right) = en_i\mathfrak{L}\lambda^{-\frac{1}{2}}e^{Y_B/2} + en_i\mathfrak{L}\lambda^{\frac{1}{2}}Y_B^{\frac{1}{2}}. \tag{15}$$

Substituting (14) into (15)

$$\frac{Y_M}{2} - 2\ln\left[\frac{\epsilon_f E_f\lambda^{\frac{1}{2}}}{en_i\mathfrak{L}} - \lambda Y_M^{\frac{1}{2}}\right] + \frac{en_i\mathfrak{L}\beta\lambda^{\frac{1}{2}}\delta}{\epsilon_f} \times\left[Y_M^{\frac{1}{2}} - \left(2\ln\left[\frac{\epsilon_f E_f\lambda^{\frac{1}{2}}}{en_i\mathfrak{L}} - \lambda Y_M^{\frac{1}{2}}\right]\right)^{\frac{1}{2}}\right] = \beta\delta E_f. \tag{16}$$

* The expression for minority carriers is true only when $e^{Y_B}\lambda^{-2} \gg Y_B$ but when large Y_M is desired this condition will be met.

In the ac-bias case the restriction on the allowable number of minority carriers ($Y - 1 > e^{Y}\lambda^{2}$) of (7) or (8) is not necessary, since lack of sufficient generation keeps the minority carrier density low regardless of the value of Y. Thus if

$$C_{si_{\min}} = \left(\frac{\partial Q}{\partial V}\right)_{Y=Y_M}$$

we have

$$C_{si_{\min}} = \frac{\epsilon_{si}\lambda^{\frac{1}{2}}}{\mathfrak{L}(Y_M - 1)^{\frac{1}{2}}}.$$

Substituting into (9) results in

$$\frac{C_{\max}}{C_{\min}} = 1 + \frac{\epsilon_f \mathfrak{L}(Y_M - 1)^{\frac{1}{2}}}{\epsilon_{si}\delta\lambda^{\frac{1}{2}}}$$

which with (16) determines the capacity ratio.

In Fig. 9, the $C_{\max}/C_{\min}$ ratio is plotted versus λ for $E_f = 3 \times 10^6$ v/cm and a 100 Å, 300 Å and 1000 Å oxide thickness. The capacity ratio decreases with the one-half power of the normalized doping density, λ, over most of the range. Investigation of the equations show that for low λ the limiting factor is the necessity of keeping the oxide from breaking down when the bands are bent toward accumulation. For the high λ

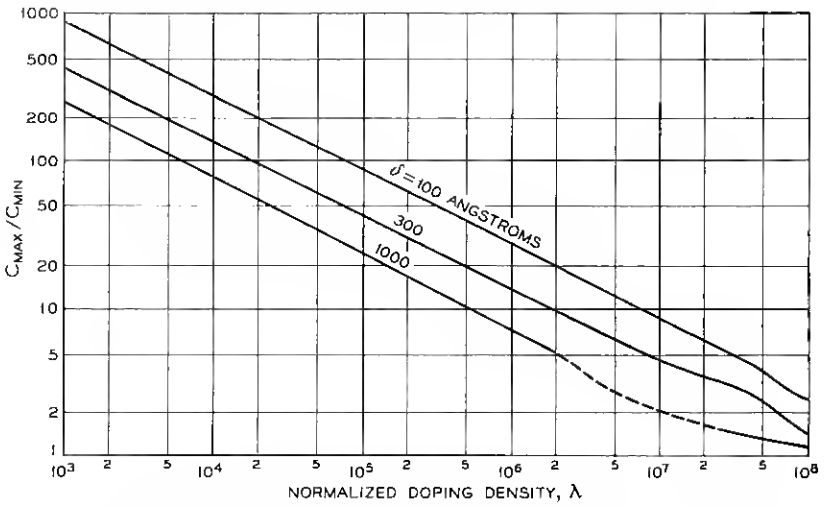

FIG. 9 — The maximum capacity ratio obtainable as a function of λ and oxide thickness for the ac-bias case. The maximum field on the oxide is 3×10^6 v/cm.

material the limiting factor is breakdown of the oxide when the bands are bent toward inversion.

In certain cases another limiting factor is encountered that is not considered in the equations, which is breakdown of the silicon itself. This occurs when the voltage carried by the silicon, Y_M/β, is greater than the avalanche breakdown voltage of a step junction whose high resistivity side is of the same resistivity as the surface varactor. An avalanche in the silicon creates sufficient minority carriers to restore true equilibrium (minority carriers terminating nearly all the field) during the part of the cycle when inversion should exist. This would increase the fraction of the applied voltage appearing across the oxide and an irreversible breakdown of the oxide might occur. Using known p^+n step junction

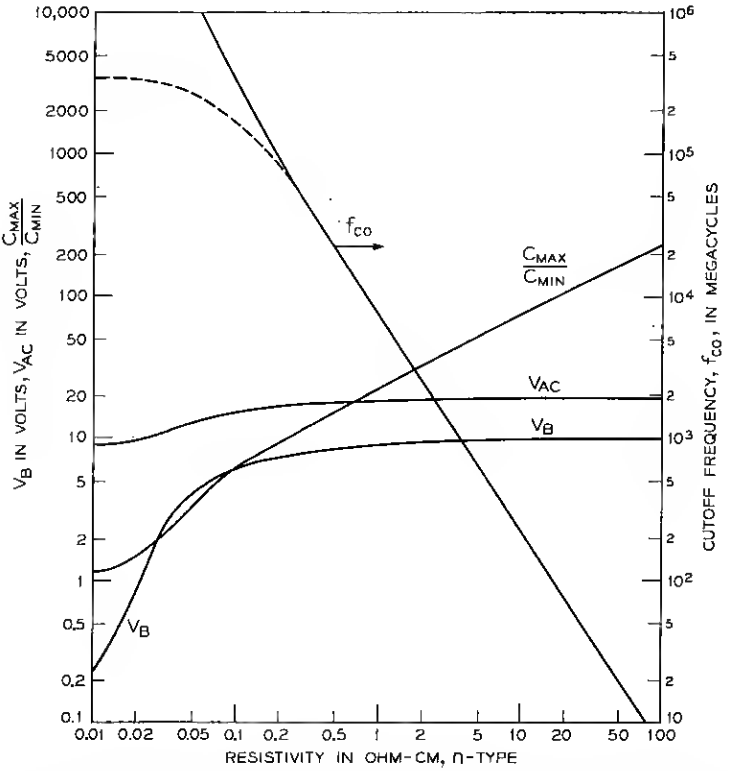

FIG. 10 — Maximum capacity ratio, C_{max}/C_{min} for ac-bias case, and the required biasing, V_B and V_{ac}, plotted against n-type resistivity. A 300 Å oxide thickness and an allowable field of 3×10^6 v/cm is used. The solid line f_{co} shows the cut-off frequency for optimum conditions of silicon thickness, while the dashed line shows the effect of adding series resistance as described in the text.

breakdown voltages[5] it was found that this was the limiting factor for a portion of the doping density range for $\delta = 1000$ Å. This range is shown as a dashed line in Fig. 9.

The maximum capacity ratio obtainable with ac biasing along with the values for optimum biasing are plotted against resistivity (n-type silicon) in Fig. 10. A 300 Å oxide thickness was assumed. The curve for cutoff frequency will be discussed in the next section.

IX. CUTOFF FREQUENCY

Assigning any one value of cutoff frequency to a varactor is difficult, since it depends upon the bias and ac signal used. Uhlir,[6] and Uenohara,[7] and Pfann[1] have offered definitions which represent the varactor as a capacity in series with a resistance. For small signal operation at a bias V_B the cutoff frequency is defined as

$$f_{co} = 1/2\pi RAC_B$$

where R is the resistance, A the area, and C_B the capacity per unit area at the bias voltage. Large ac signals cause the capacity to change appreciably during a cycle, which means that if some effective time constant is sought, it must involve a type of median capacity. The simplest solution is to determine a minimum f_{co} for any mode of operation by choosing the highest possible capacity, namely the capacity, C_f, of the oxide film. The minimum cutoff frequency is then:

$$f_{co}\,(\min) = \frac{1}{2\pi RAC_f}. \tag{17}$$

Reducing the silicon thickness increases the cutoff frequency since it decreases the resistance. However, this thickness cannot be less than $\delta(\epsilon_{si}/\epsilon_f)[(C_{max}/C_{min}) - 1]$ which is the width of the space-charge layer at maximum voltage, in order to obtain the desired capacity change. This optimum thickness may be obtained by using very thin epitaxially grown films. Table I shows the resistivity and thickness of the epitaxial

TABLE I

Epitaxial Film		C_{max}/C_{min}	Quality, Q at 1 kmc	
Resistivity	Thickness		Metal Base	0.6 mil–0.001 ohm cm Base +0.15 ohm
0.03 ohm cm	910 Å	2	5300	318
0.044	1820	3	1800	281
0.060	2730	4	890	241
0.078	3640	5	510	200

film necessary for particular capacity ratios using an optimum ac bias and assuming a 300 Å oxide. Using an operating frequency of 1000 megacycles (1 kmc), the calculated quality, Q, of the unit using the *maximum* value of capacity is tabulated for each capacity ratio for two different conditions. The first is for an epitaxial film deposited on a metal base which will give the highest possible Q. The second is for a film deposited on a 0.6 mil thick wafer of 0.001 ohm cm silicon and also assumes a 0.15 ohm package resistance ($AC_f = 2$ $\mu\mu$f). The silicon resistivity and the package resistance were chosen as representing present practical limitations.

These results are also plotted in Fig. 10, where the solid line labeled f_{co} shows the cutoff frequency for deposition on a metal base and the dashed line shows the high frequency deviation caused by adding the silicon substrate and package resistance. The optimum silicon thickness is assumed in both cases.

Experimental measurements of the capacity of a 15 ohm cm, n-type 0.002 inch thick, surface varactor were made at frequencies up to 150 mc. The unit was biased into accumulation to give the maximum capacity, which is essentially that of the oxide. From impedance considerations, this effective capacity as measured by a capacity bridge is given by

$$C_{eff} = AC/\sqrt{1 + (2\pi f RAC)^2}$$

where f is the frequency of measurement and R is the series resistance of the device. As shown in Fig. 11 the experimental points of C_{eff} versus f are well fitted by a line corresponding to AC ($=AC_{\max} \simeq AC_f$) of 3.1

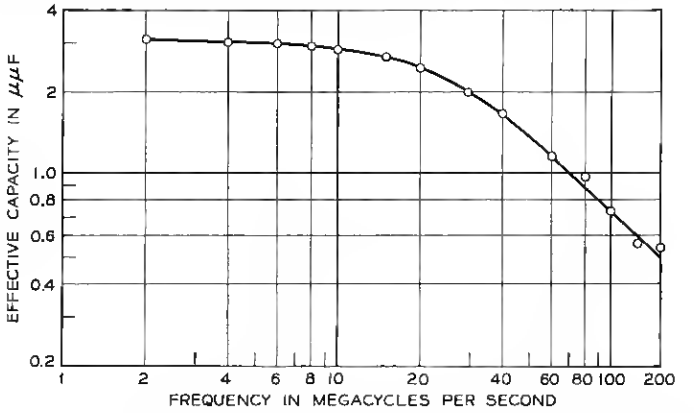

FIG. 11 — Effective capacity vs frequency for a 15 ohm cm, n-type, 0.002 inch thick, surface varactor. Experimental points lie on theoretical curve for a series RC in which $R = 2060$ ohms and $C = 3.1$ $\mu\mu$f.

$\mu\mu f$ and $R = 2060$ ohms. From Fig. 11 or (17), this device biased in the high capacity range exhibited a cutoff frequency of 25 mc. When the same device was biased in the minimum capacity range (0.15 $\mu\mu f$) it exhibited no change in effective capacity up to 150 mc.

Using a one kilomegacycle waveguide, two 0.2 ohm cm units 0.001 inch thick gave the results for capacity and resistance shown plotted against applied bias voltage in Fig. 12. From the *maximum* capacity and the corresponding resistance indicated, the calculated *minimum* cut-off frequency is 7000 mc.

To study possible frequency effects on the diclectric constant of the oxide films, capacity versus frequency measurements were carried out on an oxide grown on a heavily doped silicon crystal (.0013 ohm cm) where the contribution of the silicon space-charge capacity is negligible and the cut-off frequency is far in excess of the measuring frequencies.

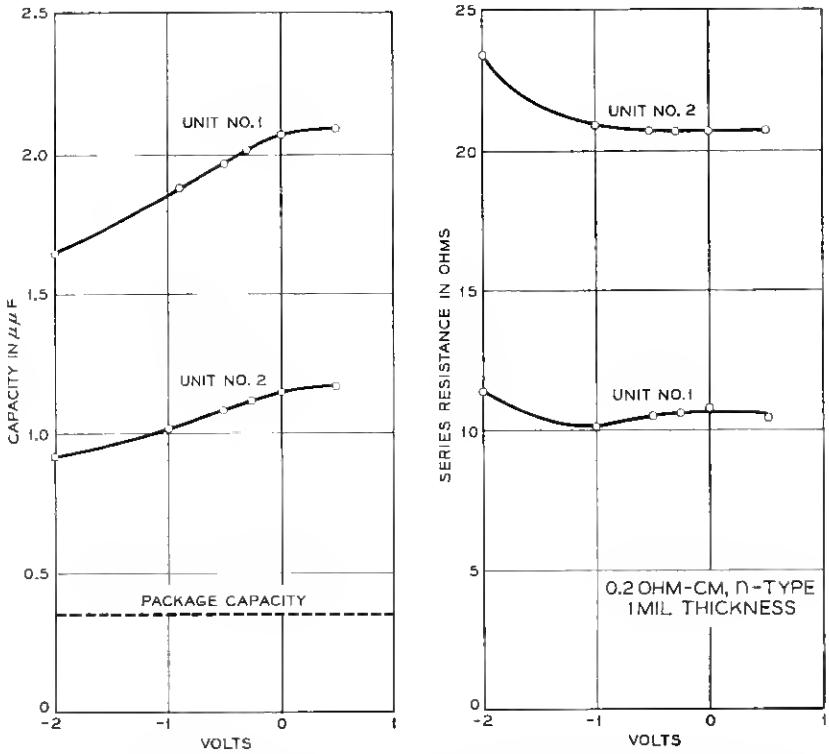

FIG. 12 — Measurements made at a 1,000 megacycle frequency for two units of 0.2 ohm cm n-type whose wafer thickness was one mil. On the left are capacity vs voltage curves and on the right are the series resistance vs voltage curves.

From the results, the dielectric constant could be represented by the relation $\epsilon = \epsilon_0(1 - 0.0465 \log_{10} f)$ where f is in megacycles and ϵ_0 is the dielectric constant at one megacycle. This relation was obtained in the range of 0.5 to 100 mc. These results are similar to those obtained for silica and other glasses.[8] If one extrapolates the above relation, the dielectric constant at 100,000 mc would still be 77 per cent of the dielectric constant at one megacycle.

X. EFFECT OF TEMPERATURE

The effect of temperature on the characteristics of the surface varactor was examined using a 0.2 ohm cm, n-type, unit with a 15 mil diameter evaporated contact. The unit was cycled between 25°C and 90.6°C and between 25°C and −73.5°C. The capacity versus voltage curves at various temperatures are shown in Fig. 13. The results indicate two points of particular interest. (1) As the theory predicts, there is little change in both maximum and minimum capacities over the above temperature range. (2) There is a lateral shift with temperatures of the capacity curves along the voltage axis (about 1 volt between −73°C and 90.6°C). Less than one-half of this shift can be accounted for by the change in contact potential (due to the shift of the Fermi level in the silicon with

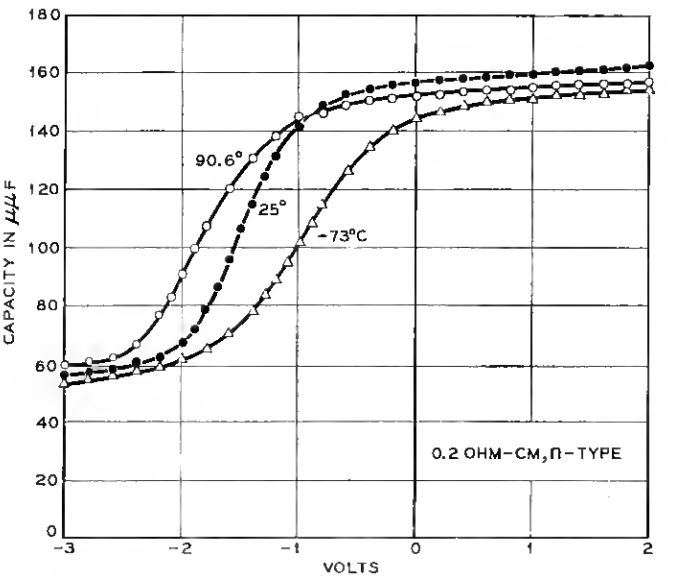

FIG. 13 — Experimental capacity vs voltage curves of a large area, 0.2 ohm cm n-type unit taken at the temperatures of 90.6°C, 25°C, and −73°C.

temperature). The remainder of the shift is not understood and is possibly associated with surface states.

XI. COMPARISON WITH STEP JUNCTION VARACTOR

Comparison of the surface varactor with the step junction varactor shows that neither device can be considered superior over the entire range of possible applications. For parametric amplifier use, the cutoff frequency, capacity ratio (amplification factor), the bandwidth, and the impedance level will effect the comparison and must all be considered. Therefore, some initial ground rules will be used to obtain a comparison, and then specific factors will be discussed which affect the comparison in various portions of the frequency range. The entire comparison is done on the basis of theory.

The ground rules are: *i.* the surface varactor is constructed of n-type silicon of optimum thickness, *ii.* the silicon dioxide layer is 300 Å thick and has a dielectric strength of 3×10^6 v/cm; *iii.* the junction varactor is constructed as a p^+n step junction whose n-type thickness is the minimum necessary to contain the space charge width; *iv.* the surface varactor is ac biased with optimum values; *v.* the junction varactor is biased from zero to the theoretical breakdown voltage; and *vi.* resistivity values refer to the n-type region of both structures. During the discussion reference will be made to Fig. 14 which shows the comparison of capacity ratio based on the cut-off frequency.

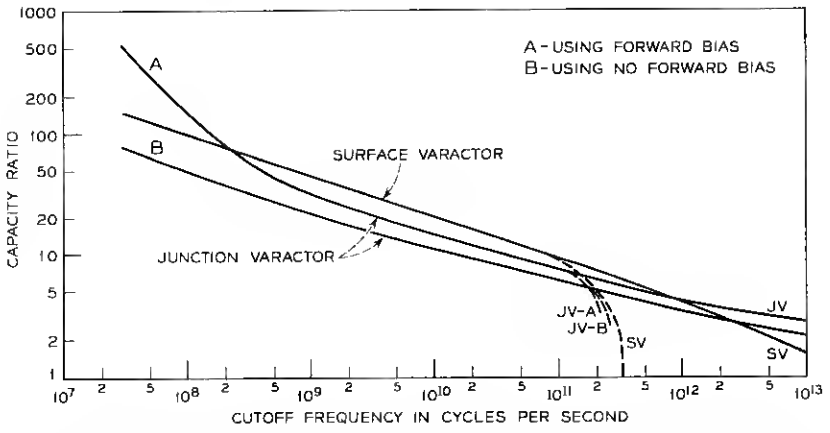

FIG. 14 — The optimum capacity ratio plotted against cutoff frequency for the surface varactor (SV) and the junction varactor (JV) using no forward bias (curve B) and using maximum allowable forward bias (curve A). The dashed lines show the deviation due to adding series resistance.

11.1 *Ultimate Frequency Range up to* 10^{12} *cps*

We will consider first that part of the frequency spectrum where both structures are made of resistivities above 0.1 ohm cm. For the assumptions used this includes cutoff frequencies up to 10^{12} cps. In this range the capacity ratio of the surface varactor is considerably higher than the junction varactor. This is because the zero-bias space-charge width of a junction is much wider than the oxide thickness, producing a higher C_{max} for the surface varactor. To a lesser degree for the surface varactor, the oxide limits the voltage on the silicon to values below that needed to cause avalanche, which keeps the C_{min} of the surface varactor from becoming as low as that of the junction varactor.

If the oxide thickness is increased to the value which allows an avalanche breakdown voltage on the silicon, it is found that the C_{max} is the same as the zero-bias capacity of the junction varactor and the capacity ratios are identical. However, if cutoff frequency is important as well as capacity ratio, the oxide thickness should always be made as *thin* as possible. For the same capacity ratio, halving the oxide thickness allows the resistivity to be halved, thus doubling the cutoff frequency. The limit on the oxide thickness should be set by the bias voltage required, but a practical lower limit of 100 Å is recommended.

Thus, in this resistivity range, the junction varactor biased from zero to the breakdown voltage can be thought of as a surface varactor with an oxide thickness of greater than 300 Å, which puts it at a disadvantage. This is shown in Fig. 14 by comparing the surface varactor with the junction varactor curve B.

11.2 *Storage Capacity in the Junction Varactor*

The use of storage capacity in the junction varactor can be of substantial benefit in the lower frequency range if the device is tailored for its use. Storage capacity in farads is given by the relation:

$$C_{st} = (q/2kT)I\tau,$$

where I is the current in amperes, and τ the lifetime of the n-type silicon in seconds. A limitation on the lifetime is that in order for the junction to recover within a cycle, the lifetime must be equal to or less than the reciprocal of the highest frequency to be used. Allowing for this, it can be shown that if the area of the junction is kept at a minimum (2×10^{-5} cm^2) and the forward current is about 5 μa, the junction varactor under optimum lifetime conditions will attain superior performance for ultimate cutoff frequencies of less than 230 mc. In Fig. 14 compare curve A of the junction varactor with that of the surface varactor. However,

for the lowest frequencies, operation in the forward-bias direction would result in a lossy device as the resistive impedance would become less than the capacitive impedance.

11.3 *High Ultimate Frequency Range*

The comparison for resistivities lower than 0.1 ohm cm is of great interest because ultrahigh cutoff frequencies are possible with both structures. The capacity ratios become equal (with a value of three) at a cutoff frequency of 2×10^{12} cps. For higher cutoff frequencies the capacity ratio of the junction varactor is higher than the surface varactor. Allowing a forward bias of 0.5 v (below that required to produce appreciable storage) the cross-over point is 6×10^{11} cps, with a $C_{max}/C_{min} = 4.6$. However, in order to take advantage of the high ultimate f_{co} the epitaxial layer thickness would have to be a few hundred angstroms. In addition, in order to maintain a reasonable circuit impedance, due to the high capacity per unit area, the diameter of the junction area would have to be less than one mil.

11.4 *Effect of Series Resistance*

If practical limitations of series resistance of the silicon substrate and the package connection are included, the surface varactor has the advantage in cutoff frequency because of the lower values of C_{max} for the surface varactor. Using a 0.6 mil thick, 0.001 ohm cm substrate and a 0.15 ohm package resistance, the cut-off frequency of junction varactor devices is maximum at 2.6×10^{11} cps for a $C_{max}/C_{min} \sim 3$. Under the same conditions the surface varactor has a 2.8×10^{11} cps f_{co} for $C_{max}/C_{min} = 3$ and a 3.2×10^{11} f_{co} for $C_{max}/C_{min} = 2$, as shown by the dashed lines of Fig. 14.

XII. ADDITIONAL COMPARISONS

There are some important differences between the structures of a practical nature. One is that the voltage across the oxide of the surface varactor must be controlled so as not to exceed its dielectric strength. The dielectric strength is normally between 3×10^6 and 10^7 volt/cm. If this value is exceeded, the device is permanently ruined. Thus, the junction varactor is considerably more rugged in regard to over voltages.

However, the oxide is also an aid since low-resistance ohmic contacts to the semiconductor are not required. Indeed, even the bottom contact can be applied to oxide. The characteristics are not affected since the area of the bottom contact is large compared to the field plate area.

This is especially true if the bottom surface is made degenerate. Elimination of the need for ohmic contacts could be quite useful for some III-V compounds like gallium arsenide, as well as silicon.

Another important practical advantage of the surface varactor is that the diffusion or alloying of junctions, which may be particularly difficult for very thin epitaxial films, is eliminated.

XIII. NONUNIFORM RESISTIVITY EFFECTS

The relations describing the capacity-voltage dependency all assumed a constant resistivity in the space-charge region. However, substantial changes in this dependency can be advantageously obtained using a varying doping level in the surface region. This might be accomplished by diffusion or epitaxy techniques. If the surface resistivity is high and gradually becomes lower going into the material, the $dC/dV \mid_{\max}$ will be lower. If the surface resistivity is low and becomes higher progressing inwards, the $dC/dV \mid_{\max}$ will be higher. This is analogous to a retrograde junction varactor. A case approximating the latter case has been calculated. This assumes a 1000 Å surface skin of 0.4 ohm cm ($\lambda^{-1} = 10^6$) on body material of 3 ohm cm ($\lambda^{-1} = 10^5$). A comparison of this case and that without the skin shows that the maximum slope dC/dV has been doubled. Tailoring the resistivity could also be used to attain a linear dependency over a large portion of the capacity charge.

XIV. COMPARISON OF SILICON AND GERMANIUM

To determine if germanium would make a better surface varactor than silicon it will be assumed that the thickness and dielectric of the oxide film is identical (as it could be for evaporated films) and the resistivity and optimum thickness are such as to produce identical cutoff frequencies. If this is done for large Y_M it can be found that the capacity ratio of the germanium varactor will be $(\epsilon_{Si}/\epsilon_{Ge})^{\frac{1}{2}}(\mu_{Ge}/\mu_{Si})^{\frac{1}{3}} = 1.17$ times the capacity ratio of the silicon varactor. For smaller Y_M (corresponds to higher cutoff frequencies) the advantage for germanium will be smaller but always greater than one. The same reasoning shows that n-type silicon is to be preferred over p-type silicon because of the higher mobility of electrons. For better varactors, the semiconductor should have a high mobility and a low dielectric constant.

XV. CONCLUSIONS

Using thermally grown oxide on silicon, experimental models of a surface varactor structure have been fabricated and tested. The experi-

mental results are in reasonable agreement with predictions of dc-bias performance, based on theoretical considerations. These calculations take into account nonequilibrium conditions existing when the period of the imposed signal is short compared to the time required for minority carrier generation.

For the structure used, it is shown that the usable capacitance ratio increases with the silicon resistivity, while at the same time the zero-bias cutoff frequency of the device decreases. For operation at higher frequencies, the device will have a cutoff frequency and a capacitance ratio close to that of a comparable p-n junction varactor operated on the reverse bias portion of its capacity-voltage characteristic. Detailed comparison of the surface varactor and the junction varactor is difficult because of the necessary assumptions regarding series resistance. These assumptions will be affected by the state of the technology and can even change the result of the comparison at high frequencies.

However, at medium frequencies the performance of the surface varactor is equivalent to the junction varactor, and at still lower frequencies is superior. The latter result follows from the larger usable capacitance ratio available in the surface varactor, since an equivalent capacitance ratio can be obtained with the junction varactor only at the expense of a large voltage swing, or by operation in the forward-bias direction, where the junction is a lossy element.

The most attractive feature of the surface varactor is its simplicity. The device can probably be fabricated without the need of a low-resistance ohmic contact to the semiconductor, and with a small active area and low capacitance. Thus, for high frequency use, in some cases where high contact resistance to the semiconductor or high capacitance is a limiting factor in the performance of a p-n junction varactor, the surface device may well prove to be superior.

It is noted that new materials and techniques, e.g., the use of thin epitaxially grown films and semiconductors other than silicon, may produce substantial increases in the cutoff frequency of the surface varactor. Therefore the comparative performance of the surface varactor and the junction varactor must be re-evaluated as these techniques, applicable to fabrication of both types of device, become available for use.

XVI. ACKNOWLEDGMENTS

Much of the material which appears in this paper is due to the discussions the author has had with R. M. Ryder and M. M. Atalla. They were instrumental both in the guidance of the experiment and in the presentation of the results.

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APPENDIX

Derivation of DC Bias Capacity

In this appendix, the capacity relations for the dc-bias case, (7) or (8), will be derived. The difficulty in carrying out this derivation rigorously is that the minority carriers (electrons in this derivation) cannot be allowed to change in number from the value attained with the dc bias alone. Therefore, simply taking the derivative of (1) to obtain capacity is not valid over the whole range of Y. However, differentiation of (1) is valid when the value of Y is such that the number of minority carriers is so small in comparison with the total charge that any change in its magnitude can be neglected. In order to make this comparison of charge contribution, expressions for the charges on minority carriers and on exposed impurities (acceptors minus holes) will be obtained. For the purpose of this discussion, p-type ($\lambda \gg 1$) will be assumed. The exposed acceptor charge is

$$Q_a = en_i\lambda \int_0^\infty (1 - e^{-y})\, dx.$$

The expression for the potential gradient dy/dx is[3]

$$\frac{dy}{dx} = \frac{2}{\mathfrak{L}} [\lambda(e^{-y} - 1) + \lambda^{-1}(e^y - 1) + (\lambda - \lambda^{-1})y]^{\frac{1}{2}}. \qquad (18)$$

For values of Y from zero to a value approximately determined by $e^Y\lambda^{-2} = Y - 1$ the second term in (18) can be neglected, and one obtains from the above relations,

$$Q_a = en_i\mathfrak{L}\lambda^{\frac{1}{2}}(Y - 1 + e^{-Y})^{\frac{1}{2}} \qquad (19)$$

The electron charge is $Q_e = Q - Q_a$ where Q is obtained from (1). Thus for the range of Y where (19) is valid we have,

$$Q_e = en_i\mathfrak{L}\lambda^{\frac{1}{2}}(e^{-Y} - 1 + Y)^{\frac{1}{2}} \left\{ \left[1 + \frac{e^Y - 1 - Y}{\lambda^2(e^{-Y} - 1 + Y)} \right]^{\frac{1}{2}} - 1 \right\}.$$

When $Y - 1 = e^Y\lambda^{-2}$, we have $e^{-y} \ll 1$ and $e^y \gg y$, so

$$Q_e = (\sqrt{2} - 1)en_i\mathfrak{L}\lambda^{\frac{1}{2}}(e^{-Y} - 1 + Y)^{\frac{1}{2}}.$$

Thus at the limit of Y where (19) is valid, Q_s is $(\sqrt{2} - 1)Q_a$. Then according to the initial premise we may write for all values of Y up to a few kT of the large positive value where $e^Y = \lambda^2(Y - 1)$,

$$C_{si} = \beta \frac{d}{dY} [en_i \mathfrak{L}\lambda^{\frac{1}{2}}(e^{-Y} - 1 + Y)^{\frac{1}{2}}]$$

or

$$C_{si} = \frac{\epsilon_{si}\lambda^{\frac{1}{2}}(1 - e^{-Y})}{\mathfrak{L}(e^{-Y} - 1 + Y)^{\frac{1}{2}}}. \tag{20}$$

At higher values of Y, where $e^Y > \lambda^2(Y - 1)$, the electron charge becomes dominant and a different approach is necessary. However, it is still the exposed acceptor charge (acceptors minus holes) which is varying with the ac signal. Therefore, the only change of charge takes place at some effective distance X_o into the semiconductor where the boundary between exposed and unexposed acceptors exists. The resulting differential capacity is, therefore, given by

$$C_{si} = \frac{\Delta Q}{\Delta V} = \frac{\epsilon_{si}}{X_o}. \tag{21}$$

For positive values of Y up to $e^Y\lambda^{-2} = Y - 1$, the effective distance X_o is, from (20) and (21),

$$X_o = \frac{\epsilon_{si}}{C_{si}} = \frac{\mathfrak{L}\lambda^{-\frac{1}{2}}(e^{-Y} - 1 + Y)^{\frac{1}{2}}}{(1 - e^{-Y})} \text{ (case of depletion)}. \tag{22}$$

For larger band bending, a region near the surface will be composed predominately of minority carriers. Let the thickness of this region be X_1, and at X_1, $y = y_1$. y_1 is determined by $y_1 - 1 = e^{y_1}\lambda^{-2}$. Now for a band bending Y at the surface, (18) gives

$$X_1 = \mathfrak{L}\lambda^{\frac{1}{2}}(e^{-y_1/2} - e^{-Y/2}). \tag{23}$$

The width of the remainder of the space-charge region X_2 is obtained from (22) by setting $Y = y_1$. The total width of the space-charge region $X_1 + X_2 = X_o$ is then given by:

$$X_o \sim \mathfrak{L}\lambda^{-\frac{1}{2}}(y_1 - 1)^{\frac{1}{2}} + \mathfrak{L}\lambda^{\frac{1}{2}}(e^{-y_1/2} - e^{-Y/2}) \text{ (case of inversion)}. \tag{24}$$

Thus a close approximation for the capacity when $Y > y_1$ is

$$C_{si} = \frac{\epsilon_{si}\lambda^{\frac{1}{2}}\mathfrak{L}^{-1}(y_1 - 1)^{\frac{1}{2}}}{y_1 - e^{-\frac{1}{2}}(Y - y_1)}.$$

Space-charge thicknesses obtained from the above approximate relation

was compared with those obtained by the alternative and more rigorous approach of numerically integrating (18). For $\lambda = 10^5$, for instance, the maximum error for C_{si} is 1.2 per cent on the low side.

LIST OF SYMBOLS

A — active area of device, cm^2
C — total capacity, farads/cm^2
C_{si} — capacity of silicon, farads/cm^2
C_f — capacity of film, farads/cm^2
C_{sc} — capacity of space charge, farads/cm^2
C_{ss} — capacity of surface states, farads/cm^2
C_B — total capacity at dc bias, farads/cm^2
d — silicon thickness, cm
E_f — maximum field to be allowed on oxide film, volts/cm
E_g — energy gap, volts
$F_{ss}(Y)$ — density of surface states, cm^{-2}
f_{co} — cut-off frequency, cps
f — frequency of measurement, cps
$\mathfrak{L}$ — $\sqrt{\dfrac{2\epsilon_{si}}{en_i\beta}} = 4.8 \times 10^{-3}$ cm
N — density of minority carriers, cm^{-3}
n_i — density of holes and of electrons in intrinsic silicon — 1.5×10^{10} cm^{-3}
n_B — density of electrons in body, cm^{-3}
Q — total charge, coul/cm^2
Q_{sc} — charge in space charge of silicon, coul/cm^2
Q_{ss} — surface state charge, coul/cm^2
Q_e — charge due to electrons, coul/cm^2
Q_a — charge due to acceptors, coul/cm^2
R — series resistance of silicon, ohms
u_B — bulk potential difference of midgap to Fermi level
V_a — applied voltage, volts
V_B — dc component of ac bias, volts
V_f — oxide film voltage, volts
V_{ac} — ac bias voltage (zero to peak)
x — distance into silicon from surface, cm
X_o — distance from surface to effective acceptor boundary, cm
Y/β — potential of surface compared to body, volts
y — potential at any distance x from the surface, kT units
y_1 — potential defined by $y_1 - 1 = e^{y_1}\lambda^{-2}$
Y_M — maximum value of surface potential, kT units

Y_B — surface potential at bias voltage, kT units
β — $e/kT = 38.5$ at room temperature
δ — oxide thickness, cm
ϵ_{si} — dielectric of silicon — 1.06×10^{-12} farads/cm
ϵ_f — dielectric of oxide — 3.4×10^{-13} farads/cm
λ — $\frac{n_i}{n_B} = \frac{p_B}{n_i}$
μ — mobility, cm^2/volt-sec
ρ — resistivity of silicon, ohm/cm
φ_m — work function of metal, volts
φ_s — strength of inversion, volts
χ — electron affinity of semiconductor

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